FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

MM74C912
6-Digit BCD Display Controller/Driver

General Description

The MM74C912 display controllers are interface elements, with memory, that drive a 6-digit, 8-segment LED display.

The display controllers receive data information through 5 data inputs A, B, C, D and DP, and digit information through 3 address inputs K1, K2 and K3.

The input data is written into the register selected by the address information when CHIP ENABLE, ($\overline{CE}$), and WRITE ENABLE, ($\overline{WE}$), are LOW and is latched when either $\overline{CE}$ or $\overline{WE}$ return HIGH. Data hold time is not required. A self-contained internal oscillator sequentially presents the stored data to a decoder where 4 data bits control the format of the displayed character and 1 bit controls the decimal point. The internal oscillator is controlled by a control input labeled OSCILLATOR ENABLE, ($\overline{OSE}$), which is tied LOW in normal operation. A high level at $\overline{OSE}$ prevents automatic refresh of the display.

The 7-segment plus decimal point output information directly drives an LED display through high drive (100 mA typ.) output drivers. The drivers are active when the control pin labeled SEGMENT OUTPUT ENABLE, ($\overline{SOE}$), is LOW and go into 3-STATE when $\overline{SOE}$ is HIGH. This feature allows for duty cycle brightness control and for disabling the output drivers for power conservation.

The MM74C912 segment decoder converts BCD data into 7-segment format.

All inputs are TTL compatible and do not clamp to the V_{CC} supply.

Features

- Direct segment drive (100 mA typ.) 3-STATE
- 6 registers addressed like RAM
- Internal oscillator and scanning circuit
- Direct base drive to digit transistor (20 mA typ.)
- Internal segment decoder
- TTL compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
MM74C912N	N28B	28-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide

Connection Diagram